Final **February 26, 1998**

Exclusively Submitted to: Communication Systems Design Magazine

Bylined Technical Article: Design of a 1 GHz RF ASIC

Editor: Nicole Westmoreland

Working Headline: Design and Simulation of an RF Transceiver ASIC

Deck: Properly simulating mixer and VCO functions in an RF ASIC can keep the designer from falling victim to those extra rounds of design iterations.

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The design of radio frequency (RF) circuits, especially an advanced RF ASIC, has long been considered black magic, rather than an exact science. Traditional RF circuit designs involve a combination of prototyping in the lab, SPICE-based simulations, and hand calculations, all of which are arduous to the design engineer and, in most cases, ultimately produce not as accurate a result as the spec calls for. But this methodology does get you in the ballpark.

Prototyping a design involves placing transistor-level functions in a test fixture for the purpose of performing measurements and constant adjustments with such external components as resistors, capacitors, and inductors. So, basically, you build up an RF single chip prototype with these external components, and all the while, you perform innumerable tweaks until you achieve the targeted performance.

Part of this traditional design approach involves SPICE-based simulation, which is acceptable for perhaps 75 percent of the design. However, certain effects such as non-linear noise and phase noise, for example, cannot be accounted for in SPICE

simulators. Consequently, effects like these and others must be either calculated by hand, utilizing simplified equations or tested in the lab. While you can achieve decent results in a test lab, they are difficult to correlate to the RF IC, itself, because the "single transistor, bond wires-on-a-test fixture" environment is considerably different.

Design and simulation of the voltage controlled oscillator (VCO) and down converting mixer functions for a 1 GHz RF transceiver ASIC represent a case in point. Applying traditional design techniques to these particular functions is like playing roulette. You can usually achieve the necessary performance, but the biggest design issue you face is over designing or placing so much margin into the design that you're foolishly investing too much current. After prototyping to get in the ballpark, you over design these functions to make sure performance meets the specification. In many conservative VCO design cases, you can meet the spec by one or two dB. However, they are considerably over designed. In other instances where a VCO design is more aggressive, the designer fails to meet the specification.

Thus, an RF ASIC designer can go through a VCO or mixer design, making wild guesses, or for that matter, even conservative guesstimates, and then when those designs are completed, he or she finds out that a redesign is necessary. The bottom line is the designer wants to save design iterations and ideally, aims for first pass design success. If that's not done, he or she will continue to incur $100,000 plus for each design iteration, plus losing up to 16 weeks to get each iteration through the fab and afterward, a month's evaluation time, not to mention lost time to market.

To properly design and simulate the mixer and VCO functions, it is important to have non-linear noise capability, which is how to measure the noise performance of a device that has frequency translation effects. A simulator like SpectreRF allows the simulation of non-linear effects through its unique algorithms. Previously, linear approximations were done to estimate these effects. These calculations are cumbersome and inaccurate by nature. The SpectreRF program allows you to quickly simulate noise figure versus all parameters such as temperature, process, power levels, and others. Advanced simulation also plays a major role in the

VCO design. Here, you still need non-linear noise capability. But you also need phase noise simulation, which is slightly different from the mixer noise figure simulation. Thus, you need the extra ability to measure phase noise of an oscillator and/or a frequency multiplier. When you use advanced simulation of this nature, you can optimize the device with considerably more confidence because your simulation is fast and highly accurate.

It is imperative, as it was in our case, that the design of a 1 GHz RF transceiver chip for a digital GSM handset not incur an endless series of design iterations in order to meet stringent consumer product time to market. The RF ASIC, figure 1, reflects that level of expeditious and efficient design, which was completed in 14 weeks with first pass success.

RF ASIC Development Flow

The system level specification is the first item in a typical RF ASIC design flow, figure 2. In our case, we use the European Telecommunications Standards Institute (ETSI) GSM specification. Given

a broad specification like this one, there is a host of different ways to implement the system. The next two blocks, system analysis and architecture choice, are usually not included in the conventional RF ASIC flow. But now, since chips are so highly integrated and are in reality, system-on-a-chip, the IC designer must be involved at this level to make sure that optimal choices and proper tradeoffs are made in order for chips to be produced correctly. At this point in the design flow, you use a combination of CAD tools and hand calculations to come up with the system analysis and architecture choice.

The architecture is then partitioned into separate chips, for instance, a transmit chip and a receiver chip or a full transmit/receive chip that operates at the RF and then another one that works at the intermediate frequency (IF). Or, the function can be split among several chips. However, the trend today is to a single RF transceiver chip. Partitioning also involves technology selection, whether or not to utilize standard CMOS, bipolar, BiCMOS, or gallium arsenide. In most cases, CMOS is used for lower frequency, while higher frequency circuitry is based on bipolar processing. These tradeoffs are determined before actually starting

the IC design. For the 1 GHz RF transceiver ASIC, our engineers used bipolar throughout the design (see box: Opting For Bipolar Over CMOS).

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At the fourth stage, you get involved with preliminary RF IC design. The system spec has by now been developed into a chip level spec, and each block inside the chip is reviewed and analyzed for topology tradeoffs or for actual selection of the optimal topology. For example, there may be two ways to design a low-noise amplifier (LNA), and you'll want to closely investigate both to achieve the best performance in this particular realm of the design.

The detailed design phase is the point where 90 percent of the work is located to make the IC a reality. You put in all the parasitics of the design, package models, and all interworkings of the IC. The design is simulated over the specified temperature range and worst case process variations to make sure the design is centered and robust. Then, you move to layout. Due to the RF IC's high frequency and high level of integration, there are crucial interactions between blocks, depending on

how they are laid out and what relative orientation they are laid out in. For this reason, this portion of the design is an art form. Currently, the majority of RF ICs continue to be laid out by hand; they are not auto routed like large digital ASICs are. So a considerable amount of care must be taken, for example, in substrate connections and in grounding. The detailed design schematic is converted into a physical implementation comprised of 24 mask layers.

Inevitably, there will be layout parasitics that can have an adverse effect on the RF performance. Therefore, parasitic extraction is performed by calculating capacitance between nodes and parasitic capacitance and resistance to the substrate. These are parasitics that couldn't be predicted before layout.

These values are calculated and are then inserted back into the detailed design schematics for a re-simulation to make sure the design is still centered and works over process and temperature variations. This represents the final simulation. The design as it is physically implemented is what is simulated, and this is the expected result after

the device is tested. Lastly, this data goes to the foundry, and after about 16 weeks, you receive the chip at which time it is evaluated and tested according to the specification.

1 GHz RF Transceiver ASIC

The bipolar RF transceiver chip consists of a low-noise amplifier (LNA), down converting mixer, intermediate frequency (IF) amplifier, I/Q demodulator, VCO, I/Q modulator, and transmit driver amplifier. On the receive side, the incoming signal is usually at a very low level, hence you need the LNA that has good power gain (about 15 dB), but a low noise figure (less than 2 dB). The down converter mixer then converts the signal from its high ≈900 MHz frequency to a lower ≈250 MHz frequency so that a considerable amount of gain can be inexpensively added with low current. This operation is performed by mixing the incoming signal with the local oscillator frequency. This local oscillator frequency is generated by phase locking the VCO with a crystal reference.

The local oscillator is offset in frequency from the RF carrier by the ≈250 MHz intermediate frequency. Those two signals go into a non-linear device (the mixer) to produce the IF at 250 MHz. The signal can then be considerably gained up because the designer has established what the receiver's noise floor is through the LNA and mixer.

In the IF strip, which is an automatic gain controlled (AGC) amplifier, the signal is gained up by as much as 90 dB depending on the power level of the incoming signal. Afterward, it goes into the I/Q demodulator stage, which converts it to baseband and splits it into real and imaginary components for processing. The processor expects two orthogonal channels, an I channel and a Q channel. The I and Q signals are then sent through and off-chip analog-to-digital converting (ADC) circuit.

There is no flexibility as far as the receiver functional blocks are concerned. But there are definitely tradeoffs on how you design each one. For instance, there are tradeoffs of power consumption versus linearity in the LNA. Assuming a constant efficiency, the more DC power you put into the LNA, the more linear its operation, therefore,

the higher the incoming signal strength it can handle.

Since the GSM handset is battery operated, you worry about DC power consumption. However, you also have to consider the strong interfering signals coming into the antenna. The desired signal must be processed in the presence of the large interfering tones. Therefore, a very linear amplifier is needed. At the same time, you want to minimize the impact on the battery. Different circuit topologies can accomplish this objective.

In our design, we chose a cascode topology with lossless series feedback, figure 3, which allowed us to optimize several parameters. First, it let us minimize the DC power consumption for a given linearity by linearizing the 1 GHz transfer function with feedback. The fact that it is lossless feedback let us maintain a low noise figure. In addition, the lossless series feedback amplifier topology allowed us to match the port impedance. The source and load of the amplifier are well-defined impedances, and you must match to them, which the feedback amplifier permitted us to do.

Aside from the advantages the topology provides, it is also a simple and efficient architecture. It comprises two transistors, hence it consumes little silicon area; it is easy to layout and has lower parasitics associated with it compared to other similar topologies.

Design tradeoffs involving power consumption versus linearity are also found in the down converting mixer. The linearity in the receiver is only as good as its weakest link. So, efficient linearity is required in every block of the receive chain, plus power consumption must be minimized in every block. An active mixer topology, figure 4, got the nod in this design because it provides efficient linearity (P_{ID} = 10 dBm), power gain (10 dB), and medium power consumption (5 mA). A bit more power is consumed in the mixer in order to get more conversion gain and linearity in the system, thus achieving a happy balance.

The modulation scheme a particular system requires determines the choice of IF amplifier and demodulator. In some cases, you can have a log amplifier with a received signal strength indicator (RSSI), or you can use an AGC amplifier with an I/Q

demodulator, which we utilized in this RF ASIC design. In either case, you're dealing with a wide range of signal powers and you need a constant output level. When the input signal is very high, the automatic gain should be reduced so that you get a constant one volt output. Conversely, if the signal source is far away, the incoming signal can be very low. In this case, automatic gain is increased to achieve the one volt output. Thus, the AGC amplifier provides -40 dB to +40 dB of gain, providing an 80 dB dynamic range.

On the transmit side, I and Q data streams are modulated together onto a carrier at an intermediate frequency (IF), which is between final frequency and baseband frequency at which digital data is clocked. In our case, we I/Q modulate the data up to an IF of about 200 MHz, utilizing a classic modulator topology. Here, you are again obviously concerned about power consumption. However, there aren't many tradeoffs in this instance. But you can still deal with power consumption by controlling chip impedance levels as best as you can and run at minimal current.

In the up-converting mixer block, the IF at about 200 MHz is converted to the transmit frequency of about 900 MHz. This frequency translation is again performed in a non-linear device; i.e., mixer. The local oscillator frequency is mixed with the IF to produce the RF frequency. The RF frequency is then filtered by an off-chip ceramic filter. The filtered signal returns on chip and is gained up to a level of +5 dBm before it goes off chip to a power amplifier and the antenna.

Power consumption in the transmit side does not pose as major an issue as it does on the receive side since the transmitter is on only about a tenth of the time, while the receiver is on virtually all of the time. Although power consumption isn't as big a concern, you still want to avoid an inordinate amount of current consumption. Linearity requires most of the design attention in the transmit side, however. In some digital modulation schemes, each component in the transistor chain must be very linear to keep from distorting the modulation and corrupting the data. Hence, highly linear and medium power consumption topologies are required.

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Box: Opting For Bipolar Over CMOS

It is true that 1 GHz RF performance is possible using CMOS and that, in most instances, CMOS is less expensive than bipolar. But the kind of CMOS that is needed for optimum RF is not as cheap as one might think. Currently, standard double poly, double metal 0.5 micron CMOS process has transistors have transition frequencies in the 15 to 20 GHz.

However, from a noise point of view, NMOS and PMOS devices have relatively high noise figures and high (MHz) $\frac{1}{F}$ noise corner. The high $\frac{1}{F}$ corner precludes designing functions like oscillators and active mixers with acceptable noise figure. This means the CMOS process will require enhancements so that it has the muscle to deliver RF frequency devices. Such improvements can include, for example, silicided gates, multiple metal layers, thick-plated metal to achieve high inductor Qs, and specialized implants to reduce the noise. In effect, what you get is a costly, but souped up CMOS process on top of a standard process, and that is what is required for CMOS to perform about 75

percent as well as a standard RF bipolar process at one GHz.

Conversely, a bipolar process is more efficient and, in our case, is cost-effective for the cost-sensitive GSM handset application. The first area to compare is device transconductance. Most functions rely on transconductance to provide their RF gain. In a bipolar device, the amount of inherent transconductance is linearly proportional to the amount of collector current that is put in it $\left(gm = \frac{Ic}{Vt} \text{ where Ic = collector current, Vt = thermal voltage} = \frac{KT}{q}\right)$. The more collector current, the more transconductance. The transconductance is very high in a biopolar device $\left(\frac{38mS}{mA}\right)$.

But in a MOS device, transconductance is not a simple function of current. It is a much more complex function of current, device size, and other factors. Subsequently, the transconductance of a MOS device is much lower than that of a bipolar device. High levels of transconductance are particularly essential for such RF functions as LNAs, active mixers, and IF amplifiers. Voltage

gain at RF is proportional to g_m x R_L, where g_m is the transconductance and R_L is the load resistance.

Furthermore, there is an issue with $\frac{1}{F}$ noise in CMOS. In an oscillator or VCO design, typically noise at the low frequency is up converted around the oscillator frequency through the non-linearities in the device. The $\frac{1}{F}$ corner is the frequency at which the noise become white. This corner is in the low kilohertz range in a bipolar device. In a MOS device, it is typically 20 to 30 MHz, which translates into a much higher VCO phase noise at low offsets from the carrier. Beyond one kilohertz offset from the carrier in a bipolar amplifier, the effects of $\frac{1}{F}$ noise are diminished. But in a MOS device, they can extend to 20 MHz, which represents another reason for using bipolar over CMOS for RF applications.

Lastly, there is the gate resistance versus base resistance problem for noise in LNAs and mixers. Base resistance in a bipolar device is relatively high, but can be easily reduced by increasing the size of a bipolar device. This, in combination with high transconductance, is not

device-size dependent and allows for excellent noise performance. In a MOS device, gate resistance is also high, but it can be reduced by making the device larger and through smarter layout. However, the number remain effectively higher than you achieve for the same type of current in a bipolar device. If exotic and costly process steps like silicided gates can be applied, then that number can be lowered, but that is not a standard process.

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Geoff Dawe Bio:

Geoff Dawe is the Director of Engineering at GHz Circuit Design, a company he founded in 1997 to develop RF IC-based products. Geoff is the author of 25 papers on RF design. He held previous positions at Alpha Industries, M/A-Com, and Analog Devices. Geoff received a BSEE from Norwich University in Vermont in 1984. He can be reached at 978-472-9727 or gcd@seacoast.com.

Figure 1. RF IC Transceiver Block Diagram

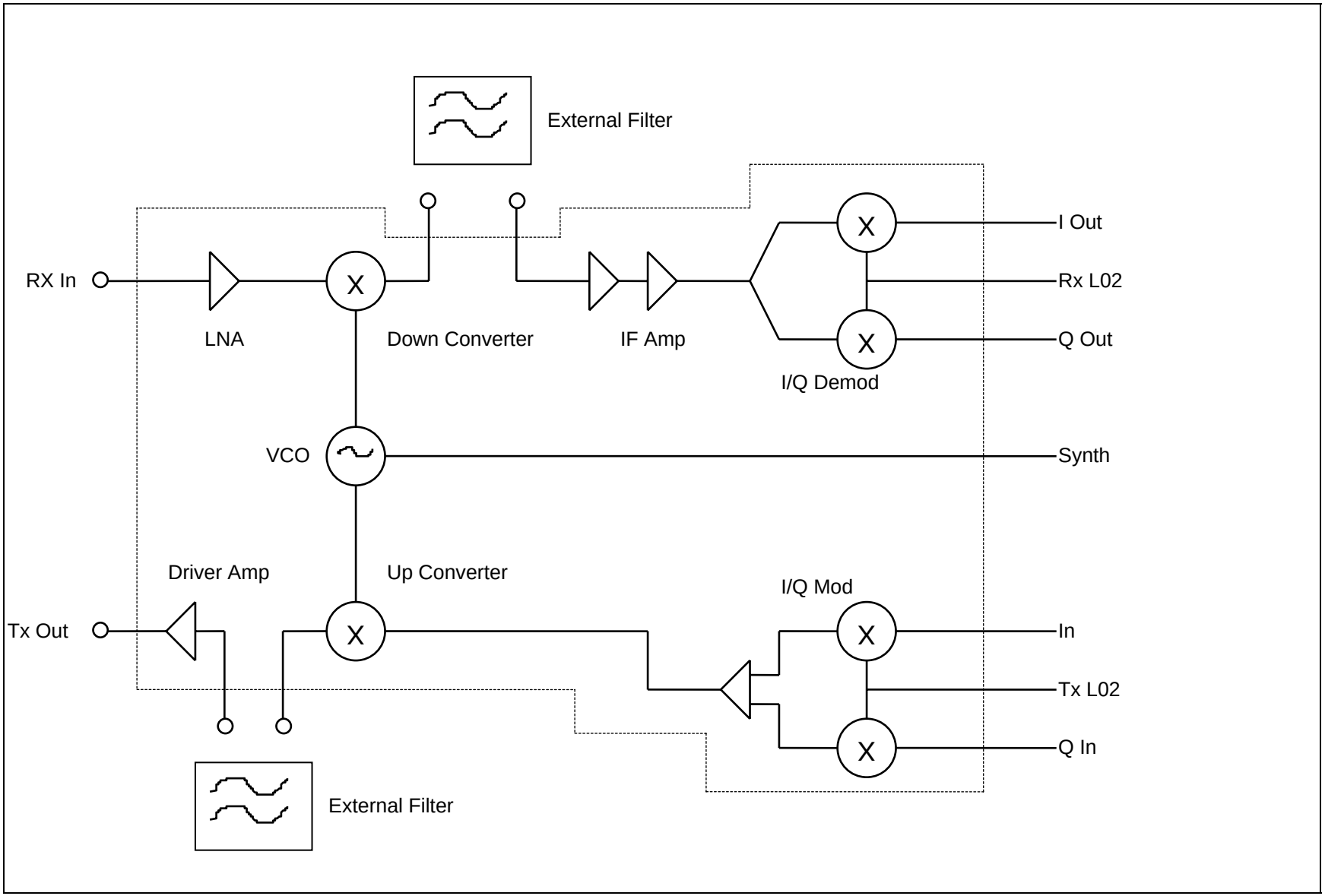

Figure 2. Typical RF ASIC Design Flow

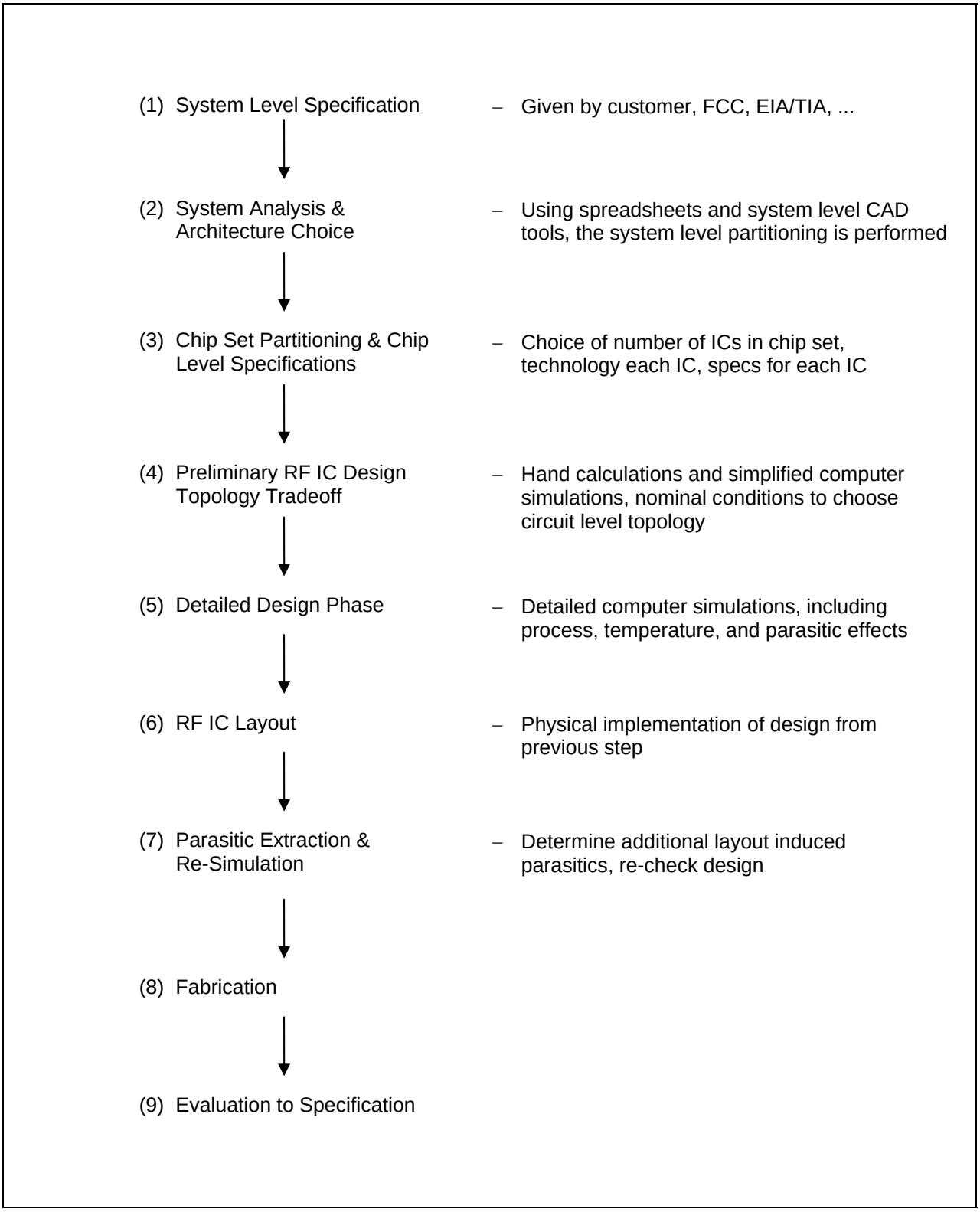

Figure 3

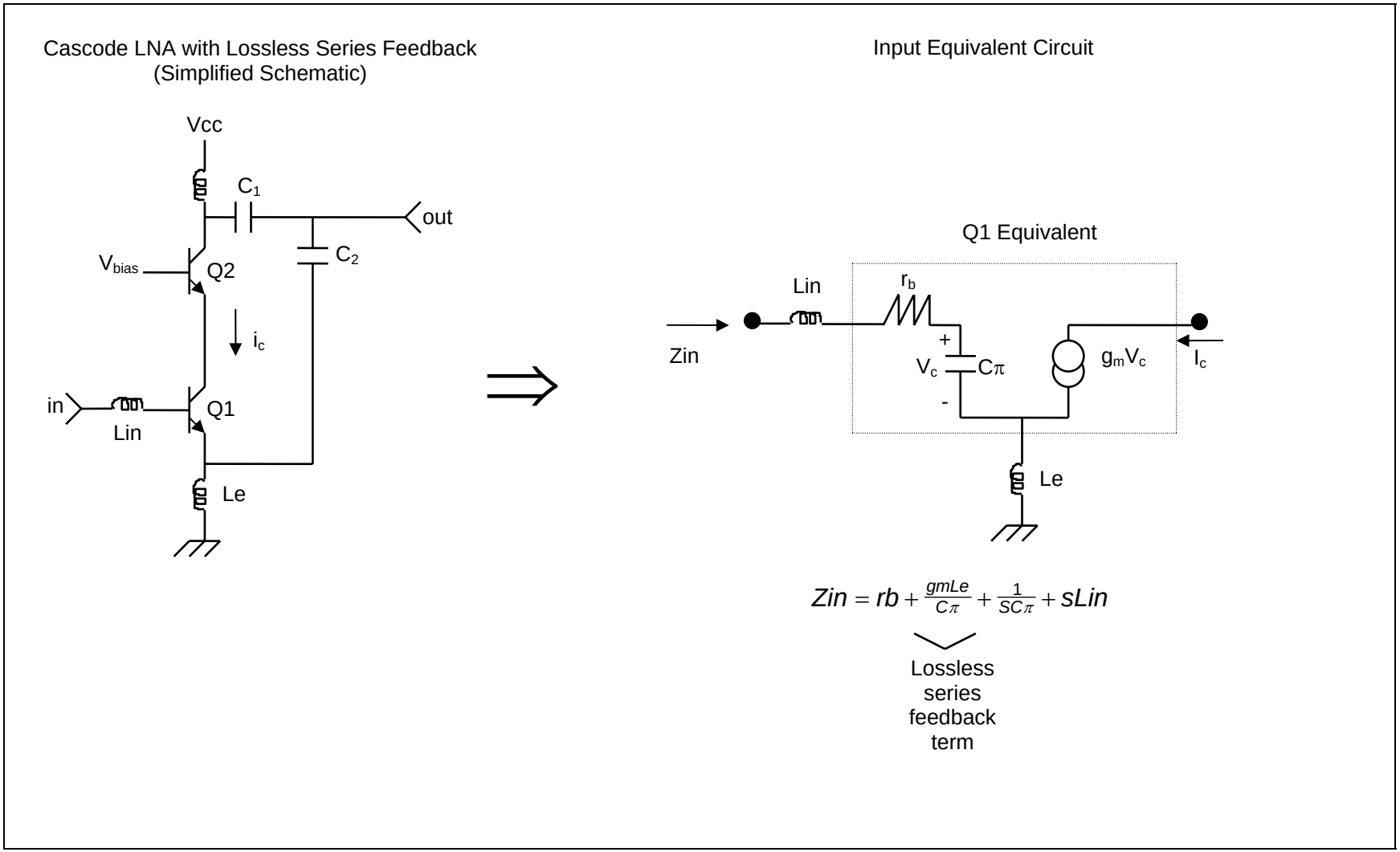
Cascode LNA with Lossless Series Feedback
(Simplified Schematic)
Vcc
C1
out
C2
Vbias
Q2
ic
in
Q1
Lin
Le
Input Equivalent Circuit
Q1 Equivalent
Lin
rb
Zin
+
Vc
Cπ
-
gmVc
Ic
Le
Zin = rb + gmLe/Cπ + 1/SCπ + sLin
Lossless
series
feedback
term

Figure 4. Active Mixer Topology